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BCM8020 PRODUCT Brief

EIGHT-CHANNEL MULTIRATE 1.0–3.2-GBPS TRANSCEIVER

FEATURES

- **Eight independent transceivers supporting multiple data rates from 1.0 Gbps to 3.2 Gbps including 1.06 Gbps, 1.25 Gbps, 2.12 Gbps, 2.488 Gbps, 2.5 Gbps, 2.667 Gbps, 3.125 Gbps, and 3.1875 Gbps**
- **Multiconfigurable to support various operating modes**
  - Eight independent 1.0- to 3.2-Gbps SerDes channels
  - Dual quad 1.0- to 3.2-Gbps SerDes with channel alignment
  - SerDes-to-SerDes retimer mode: CML and XAUI interfaces
  - Full mesh switching maps any XAUI port to any XGMII port for full redundancy on both transmitter and receiver
  - Selectable TBI DDR/RTBI or XGMII parallel interface
  - HSTL (1.8V or 1.5V) and SSTL_2 parallel interface
- **Low power dissipation**
  - Less than 300 mW per transceiver channel including I/O
- **High-performance programmable receive equalization and transmit pre-emphasis**
  - **Transmit** pre-emphasis for interoperability with CML SerDes
  - **Receive** equalization for copper interconnects
- **Enhanced test capability**
  - Serial and parallel loopback, BIST, 10G BERT, and random Ethernet packet generation
  - IEEE (1149.1) JTAG
- **Compact 23-mm × 23-mm package with no external components required**
  - No requirement for heat sink or airflow

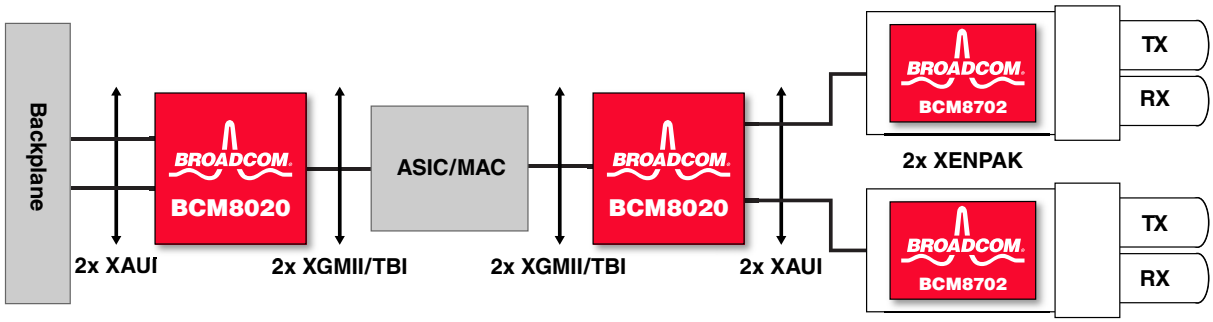
SUMMARY OF BENEFITS

- **One device supports a variety of applications including Gigabit Ethernet, 1x and 2x Fibre Channel, OC-48 SONET (with/without FEC), InfiniBand®, 10-Gigabit Ethernet, 10-Gigabit Fibre Channel, or others.**
- **Flexible architecture supports programmable configurations enabling an aggregate data transfer rate of over 20 Mbps. Built-in redundancy mode provides high availability to support critical line-side or backplane applications. The high-speed to high-speed retimer mode extends the use of longer traces on line-card designs.**
- **Advanced 0.13µ CMOS process technology provides unparalleled performance while achieving the lowest possible power consumption**
- **Eases line-card designs allowing for multiple connectors or low-cost PCB materials such as FR4**
- **Drive PMD devices or backplane directly with no external cleanup circuit required**
- **Simplifies manufacturability with integrated built-in self-test (BIST), high-speed and low-speed loopbacks, and programmable PRBS generator/checker**
- **Decreases complexity and reduces board space on multichannel line-card designs**

APPLICATIONS

- **1-Gigabit Ethernet and 10-Gigabit Ethernet LAN, MAN, WAN switches and routers**
- **1x, 2x, or 10-Gbps Fibre Channel, InfiniBand, SONET network cards**
- **Advanced test equipment (ATE)**

Two Independent Quad SerDes Application Diagram



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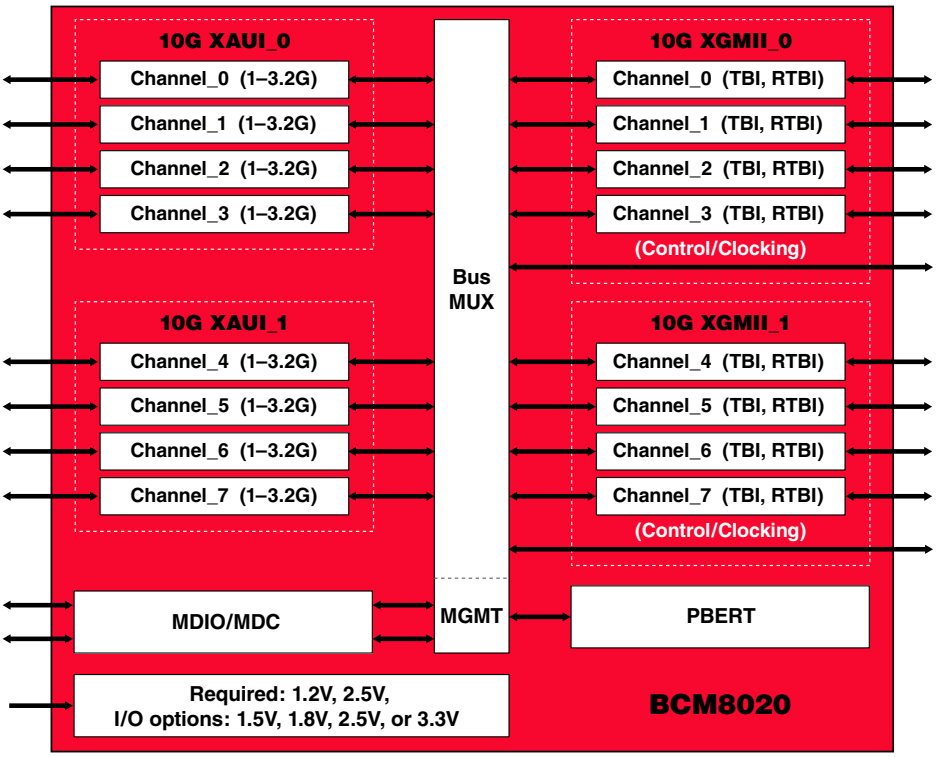
OVERVIEW



BCM8020 Block Diagram

The BCM8020 device integrates eight independent serializer/deserializer (SerDes) channels leveraging Broadcom's high-performance mixed-signal design experience along with advanced 0.13µ CMOS process technology. This, combined with a robust architecture offering the highest degree of flexibility, results in a highly programmable, lowest power SerDes solution for network line-card and backplane applications.

An internal switch connects the parallel and serial ports to enable fully redundant operation. The switch enables an active serial link to be switched to the parallel interface, while a protection serial link can be continuously monitored to ensure its condition. If the active link fails, the protection link can be instantly switched through external control to the parallel interface.

On the parallel side of the device, transmitters and receivers interface with either 5-bit (RTBI) or 10-bit (TBI) wide data on each channel or can be configured to interface to 32-bit wide data (XGMII) along with the clock and control signals. The low-speed I/O supports HSTL (1.5V or 1.8V) or SSTL_2 (2.5V) interfaces.

On the serial side of the device, transmitters and receivers support serial transmissions rates ranging from 1 Gbps to 3.2 Gbps. An on-chip phase lock loop (PLL) synthesizes the supplied reference clock to support the desired transmit rate, while clock and data recovery (CDR) units recover the receive rate clock for timing. The interface can support single-channel (octal) or dual-channel quad (XAUI) differential CML I/O.

For high-speed serial copper connections, the device incorporates both transmit pre-emphasis on the transmit channels and receive equalization on the receive channels. Transmit pre-emphasis is programmable to improve the overall cable reach and compensate for electrical imperfections associated with traces and connectors. Receive equalization provides optimal performance over a variety of receive interfaces.

Highly programmable test capabilities exist within the device to support high-speed and low-speed loopback using generators/checkers that support PRBS 27 to 231 patterns along with IEEE 802.3™ae-defined test patterns. A complete evaluation kit, including an evaluation board, related software, and documentation is available upon request.

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